

The timing diagram shows the following signal behavior:

- cla4_testbench.reset_**: High from 0ns to ~2ns, then low.
- cla4_testbench.clock**: Periodic square wave with a period of 10ns.
- cla4_testbench.a[3:0]**: 'bx at 0ns, 7 from ~2ns to ~12ns, 9 from ~12ns to ~22ns.
- cla4_testbench.b[3:0]**: 'bx at 0ns, 7 from ~2ns to ~12ns, 9 from ~12ns to ~22ns, 2 from ~22ns to ~32ns.
- cla4_testbench.cin**: High from 0ns to ~2ns, then low.
- cla4_testbench.cout**: High from 0ns to ~2ns, then low until ~12ns, then high until ~22ns, then low.
- cla4_testbench.s[3:0]**: 'bx at 0ns, E from ~2ns to ~12ns, 0 from ~12ns to ~22ns, B from ~22ns to ~32ns.

Timing diagram for the TopLevel module. The diagram shows signals over a 600ns period. TopLevel.clock is a periodic square wave. TopLevel.reset_ is a single pulse at the start. TopLevel.Q[3:0] shows a sequence of values: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D. TopLevel.q0, q1, q2, and q3 show the individual bits of the 4-bit output. TopLevel.q[3:0] shows the 4-bit output as a single signal. TopLevel.cout is a single pulse at the end of the sequence.

[illegible]

Timing diagram showing signals over 600ns. The signals are:

- TopLevel clock**: Periodic square wave.
- TopLevel reset**: Single pulse at 100ns.
- TopLevel Q[3:0]**: Hexadecimal data values: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D.
- TopLevel T**: Constant high signal.
- TopLevel q0**: Bit 0 of the data.
- TopLevel q1**: Bit 1 of the data.
- TopLevel q2**: Bit 2 of the data.
- TopLevel q3**: Bit 3 of the data.
- TopLevel q[3:0]**: Combined 4-bit data values: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D.