HIGH PERFORMANCE COMPUTER ARCHITECTURE midterm exam 30-06-2008 **MATR.NO._____**

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FIRST NAME_____

1) (34/40) Consider the following fragment of code which is executing on a VLIW processor. Initially R1=630, R2=0x1000, R3=0x3000:

```
lab:    LW      R4, 0(R2)
        LW      R5, 0(R3)
        ADD     R4, R4, R4
        ADD     R4, R4, R5
        MUL     R4, R4          ; R4=R4*R4
        SW      R4, 0(R2)
        SW      R4, 0(R3)
        ADDI    R2, R2, 4
        ADDI    R3, R3, 4
        SUBI    R1, R1, 1
        BNE     R1, R0, lab
```

Working hypothesis:

- Fetch and decode stage have a 5-instruction width
- There are two functional units for the Arithmetic-Logic operations and Branches (ALBUs) with 1 stage merged with the issue stage.
- Branches have 1 delay slot
- There are two Load/Store Units with three stages (effective address calculation, addressing, eventual read); the eventual read requires 1 clock cycle
- Write-backs can be overlapped to the decode stage
- There is one Multiplication Unit (MU) with four stages
- The register file has 24 registers R0-R23 (R0 is hardwired to the value ‘zero’)
- The register file has 5 independent input ports and 5 independent output ports
- The compiler unrolls the iterations in order to use all available registers (the number of iterations is known by the compiler – initially written in R1)

By compiling the following tables, calculate:

i) the CIT (Cycles per Iteration) of the optimally unrolled loop so that the CIT is minimized;
ii) the IPC (Instructions Per Cycle) at the end of the iterations
iii) the Utilization factor U=available_slots/total_slots

Cycle	ALBU1	ALBU2	LSU1	LSU2	MU	Comments
1	…	…	LW R4,0(R2)	LW R5,0(R3)	NOP	…
2	…	…	…	…	…	…
3	…	…	…	…	…	…

2) (6/40) Explain the difference between a Superscalar and a VLIW processor: motivate the advantages and disadvantages in each of the two cases.