CALL FOR PAPERS
Journal of Embedded Computing, IOS Press

Special Issue on
Embedded Single-Chip Multicore Architectures and related research, from System Design to Application Support
http://www.dii.unisi.it/~giorgi/jec-esc-mca/

Scope

It's now time for *scaling-out* architectures, instead of *scaling-up* frequency. As transistor count is still increasing as expected by Moore's law, recent challenges like wire-delay, design complexity, and power requirements are becoming more and more important. These problems are preventing the evolution of chip architecture in the directions followed in the previous two decades, when clock frequency as well could scale-up with Moore's law. Many researchers and companies have started to look at building multiprocessors on a single chip, following both past and novel design solutions: no doubt that we are all expecting several cores on a single chip in the near future.

Such single-chip architectures are also expected to have full success in the embedded domain. In this case, application specific requirements would also demand both computational power provided by CPU cores, high data-throughput provided by DSP cores, embedded memory, high-speed on-chip networks, but also different and novel ways to clusterize resources, and managing overall design complexity in a competitive time-to-market. In addition, low-power consumption and efficient power management are transversal constraints that should to be considered when proposing and developing such system architectures.

Clearly, this opens several new challenges for (embedded) computer architects as well as for the (embedded) experts in each of the software layers above the hardware: from run-time libraries and operating systems to applications. In particular, programmers may have to change the programming model, compilers may have to consider new ways to parallelize the application, and OS kernels might also need to handle multiple levels of parallelism. On the hardware side, an open question is: which approach would give major benefits? Tiling small cores, thinking to new organizations, or recovering many lessons learned from the past experience of multiprocessors and supercomputers?

This Special Issue aims to collect contributions related to these research questions in the embedded computing domain, taking into consideration (but not limiting to) the following topics of interest:

- Multiprocessor on-a-chip, On-Chip networks, Heterogeneous and Reconfigurable systems,
- Clustered Vectored, Multithreaded, Tiled Architectures and other novel approaches,
- Processor design, Memory Hierarchy Design, System Design, Interfacing and Security
- Managing design complexity, specification and synthesis, modeling and simulation,
- Low-Power issues, Power-aware and Adaptive Architectures,
- Operating System and Middleware support, compiler and software tools challenges,
- Architecture-aware compilation, static and run-time optimizations, workload parallelization,
- Real-Time issues, Performance modeling, Design Space Exploration,
- Case studies and practical experience reports.

Important Dates

Submission Deadline: 18 July 2005.	Final Manuscript Due: 30 September 2005.
Acceptance Notification: 12 September 2005.	Tentative Publication Date: December 2005.

Guest Editors

Roberto Giorgi and Sandro Bartolini, University of Siena, Italy.

Submission Instructions

Authors are invited to submit manuscripts reporting original unpublished contributions and recent developments following the Journal of Embedded Computing "Guide for Authors":

1) The original typescript should be submitted electronically, by preparing a TAR or ZIP folder which contains all sources (latex, figures and bibliography) together and an assembled copy of the paper in PostScript or PDF format with 5, up to 10 keywords **via email to Guest Editors**. The submission should also include the corresponding author's contact information such as email address, affiliation, etc.
2) The authors will be required to prepare their final manuscripts using either LATEX or WORD by the following author guideline: http://www.embeddedcomputing.org/IOS-authorguide.pdf . For LATEX, figures must be prepared in PostScript and appropriately incorporated into the text.
3) Papers should be limited to approximately 15 pages. A complete typescript should include, in the following order: title, author(s), address(es), abstract, keywords, introduction, text (with tables, figure captions, figures), acknowledgments, references and notes, biographical notes. At least 5 keywords are required.

Any updated information will be published on the web site: http://www.dii.unisi.it/~giorgi/jec-esc-mca/