COMPITO di ARCHITETTURA DEI CALCOLATORI del 08-07-2019 **MATRICOLA**_____

DA RESTITUIRE INSIEME AGLI ELABORATI e A TUTTI I FOGLI
→ NON USARE FOGLI NON TIMBRATI
→ ANDARE IN BAGNO PRIMA DELL'INIZIO DELLA PROVA
→ NO FOGLI PERSONALI, NO TELEFONI, SMARTPHONE/WATCH, ETC

COGNOME_____

NOME_____

SVOLGIMENTO DELLA PROVA:

☐ PER GLI STUDENTI DI "ARCHITETTURA DEI CALCOLATORI – A.A. 2015/16, 16/17, 17/18, 18/19": es. N.1+2+3+7.

NOTA: per l'esercizio 7 dovranno essere consegnati DUE files: il file del programma VERILOG e il file relativo all'output (screenshot o copy/paste)

1) [12/30] Trovare il codice assembly MIPS corrispondente al seguente programma **(usando solo e unicamente istruzioni della tabella sottostante e rispettando le convenzioni di utilizzazione dei registri dell'assembly MIPS** riportate qua sotto per riferimento).

```
double arr[20] =
{20,19,18,17,16,15,14,13,12,11,10,9,8,7,6,5,4,3,2,1};


int merge(double arr[],int l,int m,int h) {
  double arr1[11],arr2[11];
  int n1,n2,i,j,k;
  n1=m-l+1; n2=h-m;
  for(i=0; i<n1; i++) arr1[i]=arr[l+i];
  for(j=0; j<n2; j++) arr2[j]=arr[m+j+1];
  arr1[i]=9999; arr2[j]=9999;
  i=0; j=0;
  for(k=l; k<=h; k++) {
    if(arr1[i]<=arr2[j])
      arr[k]=arr1[i++];
    else
      arr[k]=arr2[j++];
  }
  return 0;
}
```

```
int merge_sort(double arr[],int low,int high) {
  int mid;
  if(low<high) {
    mid=(low+high)/2;
    merge_sort(arr,low,mid);
    merge_sort(arr,mid+1,high);
    merge(arr,low,mid,high);
  }
  return 0;
}

int main() {
  int n=20,i;
  merge_sort(arr,0,n-1);
  print_string("Sorted array: ");
  for(i=0; i<n; i++) print_double(arr[i]);
}
```

Instructions

Opcode+Funct (hexadecimal)	Instruction	Example	Meaning	Comments
00+20/00+21	**add**	`add/addu $1,$2,$3`	$1 = $2 + $3	(signed/unsigned) 3 operands; exception possible
00+22/00+23	**subtract**	`sub/subu $1,$2,$3`	$1 = $2 - $3	(signed/unsigned) 3 operands; exception possible
08/09	**add immediate**	`addi/addiu $1,$2,100`	$1 = $2 + 100	(signed/unsigned) + constant ; exception possible
00+18/00+19	**multiplication**	`mult/multu $1, $2`	Hi,Lo= $1 x $2	(signed/unsigned) 64-bit Product ; result in Hi,Lo
00+1A/00+1B	**division**	`div/divu $1, $2`	Hi= $1 % $2, Lo = $1 / $2	(signed/unsigned) division
00+10/00+12	**move from Hi / move from Lo**	`mfhi/mflo $1`	$1 = Hi ($1 = Lo)	Create copy of Hi (Create a copy of Lo)
00+2A/00+2B	**set on less than**	`slt/sltu $1,$2,$3`	if ($2 < $3) $1 = 1; else $1 = 0	(signed/unsigned) compare $2 and $3 (less than)
0A/0B	**set on less than immediate**	`slti/sltiu $1,$2,100`	if ($2 < 100) $1 = 1; else $1 = 0	(signed/unsigned) compare $2 and constant (less than)
00+24/25/26/27	**and / or / xor / nor**	`and/or/xor/nor $1,$2,$3`	$1=$2&$3 / $2|$3 / $2^$3 / !($2|$3)	3 register operands; Logical AND/OR/XOR/NOR
0C/0D/0E	**and /or / xor immediate**	`andi/ori/xori $1,$2,100`	$1 = $2 & 100 / $2 | 100 / $2 ^100	Logical AND/OR/XOR register, constant
00+00	**shift left logical**	`sll $1,$2,10`	$1 = $2 << 10	Shift left by constant
00+02/00+03	**shift right (l=logical,a=arithmetic)**	`srl/sra $1,$2,10`	$1 = $2 >> 10	Shift right by constant (for arithmetic: sign is preserved)
00+04	**shift left logical**	`sllv $1,$2,10`	$1 = $2 << $3	Shift left by variable
00+06/00+07	**shift right (l=logical,a=arithmetic)**	`srlv/srav $1,$2,10`	$1 = $2 >> $3	Shift right by variable (for arithmetic: sign is preserved)
23/20	**load word / load byte**	`lw/lb $1,100($2)`	$1 = Memory[$2+100]	Data from memory to register
24	**load byte unsigned**	`lbu $1,100($2)`	$1 = Memory[$2+100]	Data from mem. To reg.; no sign extension
2B/28	**store word / store byte**	`sw/sb $1,100($2)`	Memory[$2+100] = $1	Data from register to memory
0F	**load upper immediate**	`lui $1,0x1234`	$1=0x1234'0000	load most significant 16 bits
PSEUDOINSTRUCTION	**load address**	`la $1,var`	$1 = &var	Load address of var (lui $1,H16(&var);ori $1, L16(&var)) H16/L16=high/low 16 bits of &var
02	**jump**	`j 10000`	go to 10000	Jump to target address
00+08	**jump register**	`jr $31`	go to $31	For switch, procedure return
03	**jump and link**	`jal 10000`	$31 = PC + 4;go to 10000	For procedure call
04	**branch on equal**	`beq $1,$2,100`	if ($1 = = $2) go to PC+4+100	Equal test; PC relative branch
05	**branch on not equal**	`bne $1,$2,100`	if ($1 != $2) go to PC+4+100	Not equal test; PC relative
00+0C	**syscall**	`syscall`	call OS service $v0	See table of system calls below
10+10,rs=10	**rfe**	`rfe`	shift right (k,e) bits in STATUS reg	Exit Kernel Mode, Enable Interrupts
PSEUDOINSTRUCTION	**branch unconditional**	`b 100`	go to PC+4+100	PC relative branch (e.g., beq $0,$0,100)
PSEUDOINSTRUCTION	**no operation**	`nop`	do nothing	Do nothing (e.g. sll $0,$0,0)
30	**load-linked**	`ll $1,100($2)`	$1=Memory[$2+100]	Read and start to monitor the given memory location
38	**store-conditional**	`sc $1,100($2)`	Memory[$2+100]=$1 or →	return 0 if a coherence action happens since the previous ll ($1 must be different from 0)
11+00 fmt=10/11	**add.s / add.d**	`add.x $f0,$f2,$f4`	$f0=$f2+$f4	Single and double precision add
11+01 fmt=10/11	**sub.s / sub.d**	`sub.x $f0,$f2,$f4`	$f0=$f2-$f4	Single and double precision subtraction
11+02 fmt=10/11	**mul.s / mul.d**	`mul.x $f0,$f2,$f4`	$f0=$f2*$f4	Single and double precision multiplication
11+03 fmt=10/11	**div.s / div.d**	`div.x $f0,$f2,$f4`	$f0=$f2/$f4	Single and double precision division
11+05 fmt=10/11	**abs.s / abs.d**	`abs.x $f0,$f2`	$f0=ABS($f2)	Single and double precision absolute value
11+06 fmt=10/11	**mov.s / mov.d**	`mov.x $f0,$f2`	$f0←$f2	Single and double precision move
11+07 fmt=10/11	**neg.s / neg.d**	`neg.x $f0,$f2`	$f0= – ($f2)	Single and double precision opposite value
11+3C(31,32,3D,3E,3F) fmt=10/11	**c.lt.s / c.lt.d (ne,eq,gt,le,ge)**	`c.lt.x $f0,$f2`	Temp=($f0<$f2)	Single and double: compare $f0 and $f2 <,=,!=,>,<=>=
11+00 fmt=4/0	**move to/from coprocessor 1**	`mtc1/mfc1 $1,$f2`	$f2=$1 / $1=$f2	Move $1 to/from C1reg. $f2 (no conversion)
10+00 fmt=4/0	**move to/from coprocessor 0**	`mtc0/mfc0 $1,$2`	$c2=$1 / $1=$c2	Move $1 to/from C0 reg. $f2 (no conversion)
11+00 fmt=6/2	**move to/from control reg of cop.1**	`ctc1/cfc1 $1,$cf2`	$cf2=$1 / $1=$cf2	Move $1 to/from C1-CONTROL register
11 fmt=8,ft=1/0	**branch on true/false**	`bc1t/bc1f label`	If (Temp = = true/false) go to label	Temp is 'Condition-Code'
31/39	**load/store floating point (32bit)**	`lwc1/swc1 $f0,0($1)`	$f0←Memory[$1] / Memory[$1]←$f0	Data from FP (C1) register to memory
11+21,fmt=10/11+22,fmt=11	**convert from/to single to/from double**	`cvt.d.s/cvt s.d $f0,$f2`	$f0=(double)$f2/$f0=(single)$f2	Type conversion
11+24,fmt=11/11+20	**convert from/to single to/from integer**	`cvt.w.s/cvt s.w $f1,$f0`	$f1=(int)$f0 / $f0=(single)$f1	Type conversion

Register Usage

Name	Reg. Num.	Usage
$zero	0	The constant value 0
$s0-$s7	16-23	Saved
$t0-$t9	8-15,24-25	Temporaires
$a0-$a3	4-7	Arguments

Name	Reg.Num.	Usage
$v0-$v1	2-3	Results
$fp, $sp	30,29	frame pointer, stack pointer
$ra, $gp	31,28	return address, global pointer
$k0-$k1	26,27	Kernel usage

Reg. Num.	Usage
$f0, $f2	Return values
$f12,$f14	Function arguments
$f20,$f22,$f24,$f26,$f28,$f30	Saved registers
$f4,$f6,$f8,$f10,$f16,$f18	Temporaries registers

System calls

Service Name	Serv.No.($v0)	INPUT Arguments	OUTPUT Args
print_int	1	$a0=integer to print	---
print_float	2	$f12=float to print	---
print_double	3	($f12,$f13)=double to print	---
print_string	4	$a0=address of ASCIIZ string to print	---
read_int	5	---	$v0=integer

Service Name	Serv.No.($v0)	INPUT Arguments	OUTPUT Arguments
read_float	6	---	$f0=float
read_double	7	---	$f0-f1=double
read_string	8	$a0=address of input buffer, $a1=max chars to read	---
sbrk	9	$a0=Number of bytes to be allocated	$v0=pointer to allocated memory
exit	10	---	---

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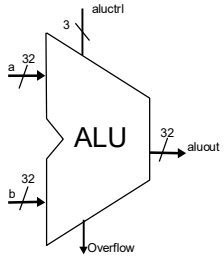
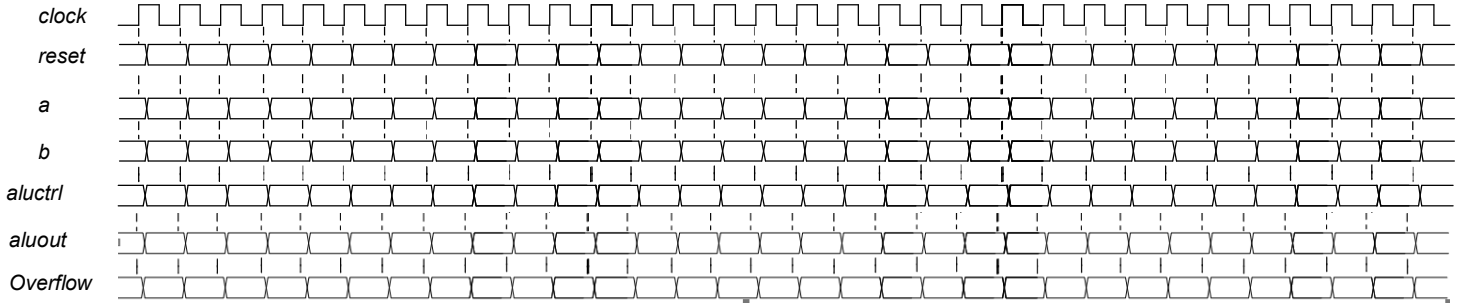
2) [5/30] Si consideri una cache di dimensione 128B e a 4 vie di tipo write-back/write-non-allocate. La dimensione del blocco e' 16 byte, il tempo di accesso alla cache e' 4 ns e la penalita' in caso di miss e' pari a 40 ns, la politica di rimpiazzamento e' FIFO. Il processore effettua i seguenti accessi in cache, ad indirizzi al byte: 626, 472, 662, 680, 639, 280, 614, 353, 321, 640, 345, 612, 585, 622, 740, 615. Tali accessi sono alternativamente letture e scritture. Per la sequenza data, ricavare il tempo medio di accesso alla cache, riportare i tag contenuti in cache al termine, i bit di modifica (se presenti) e la lista dei blocchi (ovvero il loro indirizzo) via via eliminati durante il rimpiazzamento ed inoltre in corrispondenza di quale riferimento il blocco e' eliminato.

3) [4/30] Illustrare il modo di funzionamento 2 ("rate-generator") del Timer 8254 e disegnare il diagramma temporale dei segnali CLK (clock), Counter e OUT per una data costante di tempo N.

7) [9/30] **Realizzare** in Verilog il modulo "ALU" che implementa la rete combinatoria relativa all'unità aritmetico-logica di figura che supporti le istruzioni add/sub/and/or/slt con codice di controllo (segnale aluctr) rispettivamente 2/6/0/1/7. I segnali a e b sono a 32 bit. E' gia' fornito il modulo testbench (distribuito anche su USB-drive). **Tracciare il diagramma di temporizzazione** come verifica della correttezza del modulo riportando i segnali a (32 bit), b (32 bit), aluctrl(3bit), aluout (32 bit) e Overflow. Nota: si può svolgere l'esercizio su carta oppure con ausilio del simulatore salvando una copia dell'output (diagramma temporale) e del programma Verilog su USB-drive del docente.




```
`timescale 1ns/1ps
module alu_testbench;
   reg reset_; initial begin reset_=0; #25 reset_=1; #142; $stop; end
   reg clock;  initial clock<=0;   always #5 clock<=(!clock);
   reg [31:0] a, b; reg [2:0] aluctrl;
   wire [31:0] aluout; wire Overflow;
   initial begin
      wait(reset_==1);
      // Addition unit testing
      aluctrl<=3'b010;
      @(posedge clock); a=32'h00000DEF; b=32'h00000ABC;
      @(posedge clock); a=32'h00001234; b=32'h00000105;
      @(posedge clock); a=32'h7FFFFFFF; b=32'h00000001;
      #10
      // AND unit testing
      aluctrl<=3'b000;
      @(posedge clock); a=32'h00000DEF; b=32'h00000ABC;
      @(posedge clock); a=32'h00001234; b=32'h00000105;
      @(posedge clock); a=32'h80000000; b=32'h00000001;
      #10
      // OR unit testing
      aluctrl<=3'b001;
      @(posedge clock); a=32'h00000DEF; b=32'h00000ABC;
      @(posedge clock); a=32'h00001234; b=32'h00000105;
      @(posedge clock); a=32'h80000000; b=32'h00000001;
      #10
      // Subtraction unit testing
      aluctrl<=3'b110;
      @(posedge clock); a=32'h00000DEF; b=32'h00000ABC;
      @(posedge clock); a=32'h00001234; b=32'h00000105;
      @(posedge clock); a=32'h80000000; b=32'h00000001;
      #10
      // Set Less Than unit testing
      aluctrl<=3'b111;
      @(posedge clock); a=32'h00000000; b=32'h00000DEF;
      @(posedge clock); a=32'h00001234; b=32'h00000105;
      #10 $finish;
   end
   alu MYALU(a,b,aluctrl,  aluout,Overflow);
endmodule
```



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SOLUZIONE

ESERCIZIO 1

```
.data
arr: .double 20.0,19.0,18.0,17.0
     .double 16.0,15.0,14.0,13.0
     .double 12.0, 11.0,10.0,9.0
        .double 8.0,7.0,6.0,5.0
        .double 4.0,3.0,2.0,1.0
c9999: .double 9999.0
stampa: .asciiz "Sorted array:"
.text
.globl main
#-----------------------------------
# a0=&arr,a1=l,a2=m,a3=h
# arr1+arr2 occupano 22x8=176 byte
# nel frame: sp=&arr1,t4=sp+88=&arr2
# t5=n1,t6=n2,t7=i,t8=j,t9=k
merge:
  add  $sp,$sp,-176# alloco frame
  add  $t4,$sp,88  # &arr2
  sub  $t5,$a2,$a1 # m-l
  addi $t5,$t5,1   # n1=m-l+1
  sub  $t6,$a3,$a2 # n2=h-m
  add  $t7,$0,$0   # i=0
forini1:
  slt  $t0,$t7,$t5 # i<?n1
  beq  $t0,$0,forend1
  sll  $t0,$t7,3   # i*8
  add  $t0,$sp,$t0 # &arr1[i]
  add  $t1,$t7,$a1 # l+i
  sll  $t1,$t1,3   # (l+i)*8
  add  $t1,$a0,$t1 # &arr[l+i]
  lwc1 $f4,0($t1)  # arr[l+i]
  lwc1 $f5,4($t1)
  swc1 $f4,0($t0)  # arr1[i]=
  swc1 $f5,4($t0)
  addi $t7,$t7,1   # i++
  j forini1
forend1:
  add  $t8,$0,$0   # j=0
forini2:
  slt  $t0,$t8,$t6 # j<?n2
  beq  $t0,$0,forend2
  sll  $t0,$t8,3   # j*8
  add  $t0,$t4,$t0 # &arr2[j]
  add  $t1,$t8,$a2 # m+j
  addi $t1,$t1,1   # m+j+1
  sll  $t1,$t1,3   # (m+j+1)*8
  add  $t1,$a0,$t1 # &arr[m+j+1]
  lwc1 $f4,0($t1)  # arr[m+j+i]
  lwc1 $f5,4($t1)
  swc1 $f4,0($t0)  # arr2[j]=
  swc1 $f5,4($t0)
  addi $t8,$t8,1   # j++
  j forini2
forend2:
  la   $t1,c9999   # costante 9999
  lwc1 $f4,0($t1)
  lwc1 $f5,4($t1)
  sll  $t0,$t7,3   # i*8
  add  $t0,$sp,$t0 # &arr1[i]
  swc1 $f4,0($t0)  # arr1[i]=9999
  swc1 $f5,4($t0)
  sll  $t0,$t8,3   # j*8
  add  $t0,$t4,$t0 # &arr2[j]
  swc1 $f4,0($t0)  # arr2[j]=9999
  swc1 $f5,4($t0)
  add  $t7,$0,$0   # i=0
  add  $t8,$0,$0   # j=0
  add  $t9,$0,$a1  # k=l
forini3:
  slt  $t0,$a3,$t9 # h<?k
  bne  $t0,$0,forend3
  sll  $t0,$t7,3   # i*8
  add  $t0,$sp,$t0 # &arr1[i]
  lwc1 $f4,0($t0)  # arr1[i]
  lwc1 $f5,4($t0)  #
  sll  $t0,$t8,3   # j*8
  add  $t0,$t4,$t0 # &arr2[j]
  lwc1 $f6,0($t0)  # arr2[j]
  lwc1 $f7,4($t0)  #
  sll  $t2,$t9,3   # k*8
  add  $t2,$t2,$a0 # &arr[k]
  c.le.d $f4,$f6   # arr1[]<=arr2[]
  bc1f else1
  addi $t7,$t7,1 # write arr1[i],i++
  j fineif1
else1:
  mov.d $f4,$f6    # write arr2[j]
  addi $t8,$t8,1   # j++
fineif1:
  swc1 $f4,0($t2)  # arr[k]=
  swc1 $f5,4($t2)  #
  addi $t9,$t9,1   # k++
  j forini3
forend3:
  add  $v0,$0,$0
  add  $sp,$sp,176 # dealloco frame
  jr   $ra
#-----------------------------------
# a0=&arr,a1=low,a2=high
# funzione ricorsiva: salvo ra,fp
# e a0,a1,a2 nel frame
# s0=mid va pure salvato nel frame
merge_sort:
  addi $sp,$sp,-20 # alloco frame
  sw   $a0, 0($sp)
  sw   $a1, 4($sp)
  sw   $a2, 8($sp)
  sw   $ra, 12($sp)# salvo old-ra
  sw   $s0, 16($sp)# salvo old-s0
  slt  $t0,$a1,$a2 # low<high
  beq  $t0,$0,fineif2
  add  $s0,$a1,$a2 # low+high
  srl  $s0,$s0,1   # mid=()/2
  add  $a2,$0,$s0
  jal  merge_sort
  lw   $a0,0($sp)  # &arr
  addi $a1,$s0,1   # mid+1
  lw   $a2,8($sp)  # high
  jal  merge_sort
  lw   $a0,0($sp)  # &arr
  lw   $a1,4($sp)  # low
  add  $a2,$0,$s0  # mid
  lw   $a3,8($sp)  # high
  jal  merge
fineif2:
  add  $v0,$0,$0
  lw   $a0, 0($sp) # ripristino
  lw   $a1, 4($sp)
  lw   $a2, 8($sp)
  lw   $ra, 12($sp)
  lw   $s0, 16($sp)
  addi $sp,$sp,20  # dealloco frame
  jr $ra
#-----------------------------------
# s0=n,t1=i
main:
  addi $s0,$0,20   # n
  la   $a0,arr
  add  $a1,$0,$0
  add  $a2,$s0,-1  #n-1
  jal  merge_sort
  la   $a0,stampa
  addi $v0,$0,4    # serv.4
  syscall
  add  $s1,$0,$0   # i=0
forini4:
  slt  $t1,$s1,$s0 # i<?n
  beq  $t1,$0,forend4
  sll  $t2,$s1,3   # i*8
  la   $a0,arr
  add  $t2,$t2,$a0 #&arr[i]
  lwc1 $f12,0($t2)
  lwc1 $f13,4($t2)
  addi $v0,$0,3    # serv.3
  syscall
  addi $s1,$s1,1   # i++
  j forini4
forend4:
  addi $v0,$0,10   # serv.10
  syscall
```

Console

```
Sorted array:1234567891011121314151617181920
```

ESERCIZIO 2

Sia X il generico riferimento, A=associativita', B=dimensione del blocco, C=capacita' della cache.

Si ricava S=C/B/A=# di set della cache=128/16/4=2, XM=X/B, XS=XM%S, XT=XM/S:

```
A=4, B=16, C=128, RP=FIFO, Thit=4, Tpen=40, 16 references:
=== T    X   XM  XT  XS  XB  H [SET]:USAGE [SET]:MODIF  [SET]:TAG
=== R  626   39  19   1   2  0 [1]:3,0,0,0 [1]:0,0,0,0  [1]:19,-,-,-
=== W  472   29  14   1   8  0 [1]:2,3,0,0 [1]:0,0,0,0  [1]:19,14,-,-
=== R  662   41  20   1   6  0 [1]:1,2,3,0 [1]:0,0,0,0  [1]:19,14,20,-
=== W  680   42  21   0   8  0 [0]:3,0,0,0 [0]:0,0,0,0  [0]:21,-,-,-
=== R  639   39  19   1  15  1 [1]:1,2,3,0 [1]:0,0,0,0  [1]:19,14,20,-
=== W  280   17   8   1   8  0 [1]:0,1,2,3 [1]:0,0,0,0  [1]:19,14,20,8
=== R  614   38  19   0   6  0 [0]:2,3,0,0 [0]:0,0,0,0  [0]:21,19,-,-
=== W  353   22  11   0   1  0 [0]:1,2,3,0 [0]:0,0,0,0  [0]:21,19,11,-
=== R  321   20  10   0   1  0 [0]:0,1,2,3 [0]:0,0,0,0  [0]:21,19,11,10
=== W  640   40  20   0   0  0 [0]:3,0,1,2 [0]:0,0,0,0  [0]:20,19,11,10
=== R  345   21  10   1   9  0 [1]:3,0,1,2 [1]:0,0,0,0  [1]:10,14,20,8
=== W  612   38  19   0   4  1 [0]:3,0,1,2 [0]:0,1,0,0  [0]:20,19,11,10
=== R  585   36  18   0   9  0 [0]:2,3,0,1 [0]:0,0,0,0  [0]:20,18,11,10
=== W  622   38  19   0  14  0 [0]:1,2,3,0 [0]:0,0,0,0  [0]:20,18,19,10
=== R  740   46  23   0   4  0 [0]:0,1,2,3 [0]:0,0,0,0  [0]:20,18,19,23
=== W  615   38  19   0   7  1 [0]:0,1,2,3 [0]:0,0,1,0  [0]:20,18,19,23
-------------------------------------
P1 Nmiss=13   Nhit=3  Nref=16  mrate=0.812500   AMAT=th+mrate*tpen=36.5
```

CONTENTUTI dei 4 SET al termine:

LISTA BLOCCHI USCENTI:

```
(out: XM=42 XT=21 XS=0 )
(out: XM=39 XT=19 XS=1 )

(out: XM=38 XT=19 XS=0 )
(out: XM=22 XT=11 XS=0 )
(out: XM=20 XT=10 XS=0 )
```

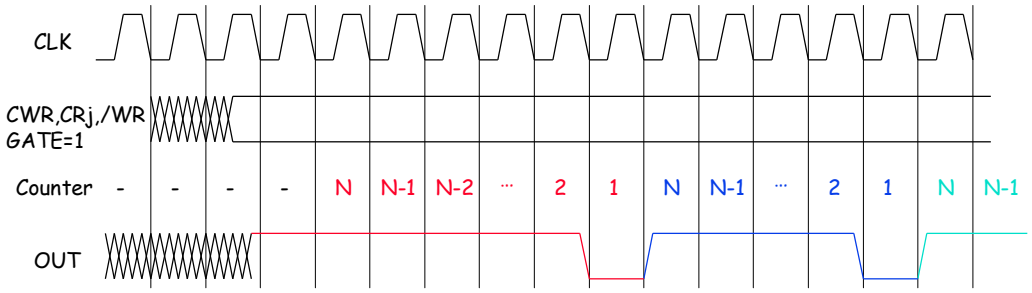
COMPITO di ARCHITETTURA DEI CALCOLATORI del 08-07-2019

SOLUZIONE

ESERCIZIO 3

Modi di conteggio

- **Modo 2: rate generator (divisore di frequenza)**
- **L'uscita è inizialmente alta e diventa bassa, per la durata di un ciclo, quando il contatore raggiunge il valore 1**



- **Si genera così un'onda quadra il cui duty-cycle è pari a (N-1)/N**
- **Se f è la frequenza del segnale di clock (CLK), la forma d'onda d'uscita (OUT) avrà frequenza f/N**

ESERCIZIO 7

Codice VERILOG:

```
module alu(a, b, aluctrl,  aluout,overflow);
   input[31:0] a, b; input[2:0] aluctrl;
   output[31:0] aluout; output overflow; reg[31:0] aluout; reg overflow;
   wire[31:0] s = a+b;
   wire[31:0] d = a-b;
   always @(aluctrl or a or b) #0.1 //re-evaluate if these change
      casex (aluctrl)
         0: begin aluout <= a & b; overflow <=0; end
         1: begin aluout <= a | b; overflow <=0; end
         2: begin aluout <= s; overflow <= (a[31] == b[31]) & (a[31] != s[31]); end
         6: begin aluout <= d; overflow <= (a[31] != b[31]) & (a[31] != d[31]); end
         7: begin aluout <= a<b ? 1:0; overflow <=0; end
         default: aluout<=0; //default to 0, should not happen
      endcase
endmodule
```

Diagramma temporale: